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EXAMINER	
HOGUE, DENNIS A	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/673,775	MABUCHI, KEIJI	
	Examiner	Art Unit	
	DENNIS HOGUE	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 September 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *4/2/2007*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This is the initial Office Action based on the 10/673775 application filed 9/29/2003. Claims 1-26, as originally filed, are currently pending and have been considered below.

Drawings

2. Figures 11 and 12 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-4, 6-9, 12, and 20-23 are rejected under 35 U.S.C. 102(b) as being anticipated by Mori et al. (US Patent 7,102,680).

Regarding claim 1, Mori et al. teach a solid-state image pickup device [105, Fig.1] (CCD, col. 3 lines 50-55), comprising: a plurality of photoelectric conversion sections [401, 403, Fig. 3] (the shallow p-well and photoelectric conversion region form a photodiode, col. 6 lines 7-11; a plurality of these color components are arranged in a mosaic pixel by pixel at the image forming surface of the CCD, col. 3 lines 55-58; and convert the light to a color signal by photoelectric conversion, col. 3 line 51 to col. 4 line 8; also see Fig. 3 for a diagram of an individual pixel) provided in a semiconductor layer [400, Fig. 3] (the pixels are formed on a semiconductor substrate, col. 6 lines 7-11); a transfer switch [404-408, Fig. 3] (buried channel, transfer electrode or gate, insulating layer, channel stop region, and transfer gate region, col. 6 lines 12-21) provided adjacent said photoelectric conversion sections in said semiconductor layer (see Fig. 3; the photoelectric conversion area 403 is adjacent to the transfer switch 404-408) for transferring charge from said photoelectric conversion sections (the transfer gate region 408 is placed between the photoelectric conversion region 403 and the buried channel 404 to control the transfer of charge from the photoelectric conversion region to the buried channel, col. 4 lines 41-46, col. 6 lines 19-22); and means for applying a predetermined voltage to said semiconductor layer [202, Fig. 1] (the substrate bias controller 202 sets the substrate bias voltage Vsub at different values in the normal driving mode and the n-addition driving mode, col. 5 lines 63-67) within a period which includes at least part of a transfer period of said transfer switch (in normal driving mode,

the substrate bias is set to 9 volts; in n-addition driving mode, the substrate voltage is set to a different value as determined by the value of n, col. 7 lines 36-43; in either case, charge is transferred from the pixel elements and out of the CCD, col. 7 lines 44-47; therefore, a predetermined voltage is applied to the substrate within a period which includes at least part of a transfer period of the transfer switch, i.e. it is applied for the whole transfer period of the transfer switch).

Regarding claim 2, Mori et al. teach the solid-state image pickup device according to claim 1, wherein the predetermined voltage shallows the potential in charge storage regions of said photoelectric conversion sections (the substrate bias voltage Vsub is used to determine the overflow level OFL of the charge accumulating portion, col. 4 lines 52-55; the examiner interprets the phrase "shallows the potential in charge storage regions" to mean that the barrier potential of the charge storage region is reduced; this is analogous to the phrase "decrease the overflow level" as per Mori et al.).

Regarding claim 3, Mori et al. teach a solid-state image pickup device, comprising: a plurality of photoelectric conversion sections provided in a semiconductor layer (see the explanation regarding claim 1); and means for applying a first voltage (12.2 volts, col. 6 lines 41-54) and a second voltage different from the first voltage (9 volts, a reference voltage, col. 6 lines 41-54) to said semiconductor layer (in normal driving mode, the substrate bias is set to 9 volts; in n-addition driving mode, the substrate voltage is set to a different value as determined by the value of n, col. 7 lines 36-43; for example, when n=2, Vsub=12.2 volts, col. 6 lines 41-54) within a period

including at least part of a charge storage period of said photoelectric conversion section (in either case, charge is transferred from the pixel elements and out of the CCD, col. 7 lines 44-47; therefore, a predetermined voltage is applied to the substrate within a period which includes at least part of a transfer period of the transfer switch, i.e. it is applied for the whole transfer period of the transfer switch).

Regarding claim 4, Mori et al. teach the solid-state image pickup device according to claim 3, wherein the first voltage (12.2 volts) shallows the potential in charge storage regions of said photoelectric conversion sections more than the second voltage (9 volts) (the substrate bias voltage Vsub is used to determine the overflow level OFL of the charge accumulating portion, col. 4 lines 52-55; the examiner interprets the phrase "shallows the potential in charge storage regions" to mean that the barrier potential of the charge storage region is reduced; this is analogous to the phrase "decrease the overflow level" as per Mori et al.; increasing the absolute value of the substrate bias voltage enables the overflow level to be decreased; in this case, the barrier potential when Vsub=12.2 V will be less than the barrier potential when Vsub=9 V).

Regarding claim 6, Mori et al. teach a solid-state image pickup device [105, Fig.1] (CCD, col. 3 lines 50-55), comprising: a semiconductor substrate [400, Fig. 3] (n-type semiconductor substrate, col. 6 lines 7-11) having a well region formed thereon [401, 402, Fig. 3] (shallow p-well first region 401, deep p-well second region 402, and other elements formed thereon as shown in Fig. 3, see col. 6 lines 7-9); a photoelectric conversion element formed in said well region for receiving light and producing signal

charge in accordance with an amount of the received light [401, 403, Fig. 3] (the shallow p-well 401 and photoelectric conversion region 403, which is inherently an n-type region, form a photodiode, col. 6 lines 7-11; which converts the light to a color signal by photoelectric conversion, col. 3 line 51 to col. 4 line 8; also see Fig. 3 for a diagram of an individual pixel); a readout section formed in said well region [404-408, Fig. 3] (buried channel, transfer electrode or gate, insulating layer, channel stop region, and transfer gate region, col. 6 lines 12-21) for reading out the signal charge produced by said photoelectric conversion element (the transfer gate region 408 is placed between the photoelectric conversion region 403 and the buried channel 404 to control the transfer of charge from the photoelectric conversion region to the buried channel, col. 4 lines 41-46, col. 6 lines 19-22) at a predetermined readout timing (driving control of the CCD 105 is performed using various driving signals including charge transfer pulse TG, col. 4 lines 32-35); and voltage control means [202, Fig. 1] (the substrate bias controller 202 sets the substrate bias voltage Vsub at different values in the normal driving mode and the n-addition driving mode, col. 5 lines 63-67) for applying a predetermined substrate bias voltage to said well region upon reading out of the signal charge by said readout section (in normal driving readout mode, the substrate bias is set to 9 volts; in n-addition driving readout mode, the substrate voltage is set to a different value as determined by the value of n, col. 7 lines 36-43; for example, when n=2, Vsub=12.2 volts, col. 6 lines 41-54; normal readout mode is a mode where a single pixel is desired to be read out, and n-addition readout mode is a mode where n pixels are combined and read out together for fast readout, col. 4 line 65 to col. 5 line 9).

Regarding claim 7, Mori et al. teach the solid-state image pickup device according to claim 6, wherein said photoelectric conversion element is provided for each of a plurality of pixels formed in a two-dimensional array on said semiconductor substrate (a plurality of color components are arranged in a mosaic pixel by pixel at the image forming surface of the CCD, col. 3 lines 55-58; and convert the light to a color signal by photoelectric conversion, col. 3 line 51 to col. 4 line 8; also see Fig. 3 for a diagram of an individual pixel; the pixels are formed on a semiconductor substrate, col. 6 lines 7-11; the CCD is an interline CCD, col. 6 lines 4-6; the CCD uses horizontal and vertical driving pulses, col. 4 lines 32-35; therefore, it is a two dimensional array of pixels).

Regarding claim 8, Mori et al. teach the solid-state image pickup device according to claim 7, wherein said well region is formed electrically integrally in a region of said semiconductor substrate (the well region 401 is formed electrically integrally in a region of semiconductor substrate 400, see Fig. 3) which includes all of said pixels arranged in the two-dimensional array (all of the pixels of the two dimensional array are formed on the substrate, see Fig. 3 and col. 6 lines 7-18), and a common substrate bias voltage to all of said pixels is applied to the well regions (the substrate bias controller 202 sets the substrate bias voltage Vsub, col. 5 lines 63-67; all of the pixels are formed on the substrate, therefore the same substrate voltage is applied to all pixels).

Regarding claim 12, Mori et al. teach the solid-state image pickup device according to claim 6, wherein said solid-state image pickup device is a charge-coupled devices type solid-state image pickup device (the device is an interline CCD, col. 6 lines

4-11) which includes a plurality of pixels each of which includes said photoelectric conversion element (photoelectric conversion region 403, col. 6 lines 4-11), a charge transfer section for fetching and successively transferring the signal charge produced by the photoelectric conversion elements of said pixels (transfer gate region 408, col. 6 lines 12-29), and a common conversion section for successively converting the signal charge successively transferred by said charge transfer section into an electric signal (interline CCDs inherently have a common conversion section to convert the charges to voltage; vertical and horizontal registers shift charge packets from the individual pixels to a common conversion section that converts the charges to a voltage signal; this is necessary so that subsequent circuitry can process the information).

Regarding claim 20, Mori et al. teach a driving method for a solid-state image pickup device (method for driving an interline CCD, col. 6 lines 4-11) wherein a photoelectric conversion element for receiving light and producing signal charge in accordance with an amount of the received light [401, 403, Fig. 3] (the shallow p-well and photoelectric conversion region form a photodiode, col. 6 lines 7-11; a plurality of these color components are arranged in a mosaic pixel by pixel at the image forming surface of the CCD, col. 3 lines 55-58; and convert the light to a color signal by photoelectric conversion, col. 3 line 51 to col. 4 line 8; also see Fig. 3 for a diagram of an individual pixel) and a readout section [404-408, Fig. 3] (buried channel, transfer electrode or gate, insulating layer, channel stop region, and transfer gate region, col. 6 lines 12-21) for reading out the signal charge produced by said photoelectric conversion element (the transfer gate region 408 is placed between the photoelectric conversion

region 403 and the buried channel 404 to control the transfer of charge from the photoelectric conversion region to the buried channel, col. 4 lines 41-46, col. 6 lines 19-22) at a predetermined readout timing (driving control of the CCD 105 is performed using various driving signals including charge transfer pulse TG, col. 4 lines 32-35) are provided in a well region formed on a semiconductor substrate [401, 402, Fig. 3] (shallow p-well first region 401, deep p-well second region 402, and other elements formed thereon as shown in Fig. 3, col. 6 lines 7-9), comprising a step of applying a predetermined substrate bias voltage to said well region upon reading out of the signal charge by said readout section (in normal driving readout mode, the substrate bias is set to 9 volts; in n-addition driving readout mode, the substrate voltage is set to a different value as determined by the value of n, col. 7 lines 36-43; for example, when n=2, Vsub=12.2 volts, col. 6 lines 41-54; normal readout mode is a mode where a single pixel is desired to be read out, and n-addition readout mode is a mode where n pixels are combined and read out together for fast readout, col. 4 line 65 to col. 5 line 9).

Regarding claim 21, Mori et al. teach the driving method for a solid-state image pickup device according to claim 20, wherein said photoelectric conversion element is provided for each of a plurality of pixels formed in a two-dimensional array on said semiconductor substrate (a plurality of color components are arranged in a mosaic pixel by pixel at the image forming surface of the CCD, col. 3 lines 55-58; and convert the light to a color signal by photoelectric conversion, col. 3 line 51 to col. 4 line 8; also see Fig. 3 for a diagram of an individual pixel; the pixels are formed on a semiconductor substrate, col. 6 lines 7-11; the CCD is an interline CCD, col. 6 lines 4-6; the CCD uses

horizontal and vertical driving pulses, col. 4 lines 32-35; therefore, it is a two dimensional array of pixels).

Regarding claim 22, Mori et al. teach the driving method for a solid-state image pickup device according to claim 21, wherein said well region is formed electrically integrally in a region of said semiconductor substrate (the well region 401 is formed electrically integrally in a region of semiconductor substrate 400, see Fig. 3) which includes all of said pixels arranged in the two-dimensional array (all of the pixels of the two dimensional array are formed on the substrate, see Fig. 3 and col. 6 lines 7-18), and a common substrate bias voltage to all of said pixels is applied to the well regions (the substrate bias controller 202 sets the substrate bias voltage Vsub, col. 5 lines 63-67; all of the pixels are formed on the substrate, therefore the same substrate voltage is applied to all pixels).

Regarding claims 9 and 23, Mori et al. teach the driving method for a solid-state image pickup device according to claims 7 and 21, wherein said well region is formed in an electrically isolated relationship for each row of said pixels arranged in the two-dimensional array (the well region is inherently formed in an electrically isolated relationship for each row of said pixels arranged in the two dimensional array; the pixels of one row must be isolated from the pixels in adjacent rows, otherwise photometric data could not be collected and distinguished for each pixel area and an image could not be detected), and an independent substrate bias voltage is applied to the cell regions for each row (the substrate bias controller 202 sets the substrate bias voltage

Vsub, col. 5 lines 63-67; the substrate bias voltage is independent of other voltages and is applied to all pixels constructed on the substrate).

5. Claims 13-16, 19, and 25-26 are rejected under 35 U.S.C. 102(b) as being anticipated by Morimoto (US Patent 5,729,287).

Regarding claim 13, Morimoto teaches a solid-state image pickup device (solid state image pick-up device, col. 1 lines 7-8), comprising: a semiconductor substrate [111, Fig. 2] (n-type semiconductor substrate, col. 1 lines 28-29) having a well region formed thereon [112, Fig. 2] (p-type impurity well layer and other elements formed thereon as shown in Fig. 2, col. 1 lines 28-29); a photoelectric conversion element formed in said well region for receiving light and producing signal charge in accordance with an amount of the received light [101, Fig. 1; 112, 113, Fig. 2] (a photodiode 101 is formed from the p-type impurity well layer 112 and the n-type impurity layer 113, col. 1 lines 29-34); a readout section [118, 119, 120, Fig. 2] (readout gate region 118, insulation layer 119, and vertical transfer electrode 120, col. 1 lines 38-41, 46-50) formed in said well region for reading out the signal charge produced by said photoelectric conversion element (the vertical transfer electrode 120 serves as a control electrode for switching the readout gate region 118 ON and OFF, col. 1 lines 50-53) at a predetermined readout timing [Fig. 6] (a read out pulse Vr is applied to vertical transfer electrode 120, and the overall charge accumulated in the photodiode 101 is read out to the vertical CCD register 102, col. 8 lines 6-10); and voltage control means (clock, col. 7 lines 46-52) for applying a substrate bias voltage to said well region [Fig. 6] (during a

period Pa, a substrate voltage VSUBa is applied, col. 7 line 58) and changing the substrate bias voltage during a storage period of the signal charge by said photoelectric conversion element (in a subsequent period Pb, a substrate voltage VSUBb which is lower than the substrate voltage VSUBa is applied, col. 7 lines 66-67; Figs. 6 and 7A-7C clearly show that the voltage change happens during the storage period of the photodiode).

Regarding claim 14, Morimoto teaches the solid-state image pickup device according to claim 13, wherein said photoelectric conversion element is provided for each of a plurality of pixels formed in a two-dimensional array on said semiconductor substrate [101, Fig. 1] (photodiodes 101 are provided for each pixel, and the plurality of photodiodes form a two-dimensional array of pixels on the CCD, col. 1 lines 13-24).

Regarding claim 15, Morimoto teaches the solid-state image pickup device according to claim 14, wherein said well region is formed electrically integrally in a region of said semiconductor substrate (a p-type impurity well layer 112 is formed on an n-type semiconductor substrate 111, col. 1 lines 28-29) which includes all of said pixels arranged in the two-dimensional array (all of the photodiodes 101 are formed on the substrate, col. 1 lines 15-34), and a common substrate bias voltage to all of said pixels is applied to the well regions (substrate voltages VSUBa and VSUBb are applied to the substrate, col. 7 lines 58-67; all of the pixels are formed on the substrate, therefore the same substrate voltage is applied to all pixels).

Regarding claim 16, Morimoto teaches the solid-state image pickup device according to claim 14, wherein said well region is formed in an electrically isolated

relationship for each row of said pixels arranged in the two-dimensional array (the well region is inherently formed in an electrically isolated relationship for each row of said pixels arranged in the two dimensional array; the pixels of one row must be isolated from the pixels in adjacent rows, otherwise photometric data could not be collected and distinguished for each pixel area and an image could not be detected), and an independent substrate bias voltage is applied to the cell regions for each row (substrate voltages VSUBa and VSUBb are applied to the substrate, col. 7 lines 58-67; the substrate bias voltage is independent of other voltages and is applied to all pixels constructed on the substrate).

Regarding claim 19, Morimoto teaches the solid-state image pickup device according to claim 13, wherein said solid-state image pickup device is a charge-coupled devices type solid-state image pickup device (CCD type solid state image pick-up device, col. 1 lines 6-7) which includes a plurality of pixels [106, Fig. 1] each of which includes said photoelectric conversion element (unit pixel 106 comprises a photodiode 101, col. 1 lines 15-24), a charge transfer section for fetching and successively transferring the signal charge produced by the photoelectric conversion elements of said pixels [102, 103, Fig. 1] (vertical CCD registers 102 and horizontal CCD register 103, col. 1 lines 15-24), and a common conversion section for successively converting the signal charge successively transferred by said charge transfer section into an electric signal [104, Fig. 1] (charge detecting portion 104 detects the charge transferred from the horizontal CCD register, col. 1 lines 15-24).

Regarding claim 25, Morimoto teaches a driving method for a solid-state image pickup device (driving method for driving a solid state image pick-up device, see title) wherein a photoelectric conversion element for receiving light and producing signal charge in accordance with an amount of the received light [101, Fig. 1; 112, 113, Fig. 2] (a photodiode 101 is formed from the p-type impurity well layer 112 and the n-type impurity layer 113, col. 1 lines 29-34) and a readout section [118, 119, 120, Fig. 2] (readout gate region 118, insulation layer 119, and vertical transfer electrode 120, col. 1 lines 38-41, 46-50) for reading out the signal charge produced by said photoelectric conversion element (the vertical transfer electrode 120 serves as a control electrode for switching the readout gate region 118 ON and OFF, col. 1 lines 50-53) at a predetermined readout timing [Fig. 6] (a read out pulse Vr is applied to vertical transfer electrode 120, and the overall charge accumulated in the photodiode 101 is read out to the vertical CCD register 102, col. 8 lines 6-10) are provided in a well region [112, Fig. 2] (p-type impurity well layer and other elements formed thereon as shown in Fig. 2, col. 1 lines 28-29) formed on a semiconductor substrate [111, Fig. 2] (n-type semiconductor substrate, col. 1 lines 28-29), comprising a step of applying a substrate bias voltage to said well region [Fig. 6] (during a period Pa, a substrate voltage VSUBa is applied, col. 7 line 58) and changing the substrate bias voltage during a storage period of the signal charge by said photoelectric conversion element (in a subsequent period Pb, a substrate voltage VSUBb which is lower than the substrate voltage VSUBa is applied, col. 7 lines 66-67; Figs. 6 and 7A-7C clearly show that the voltage change happens during the storage period of the photodiode).

Regarding claim 26, Morimoto teaches the driving method for a solid-state image pickup device according to claim 25, wherein said photoelectric conversion element is provided for each of a plurality of pixels formed in a two-dimensional array on said semiconductor substrate [101, Fig. 1] (photodiodes 101 are provided for each pixel, and the plurality of photodiodes form a two-dimensional array of pixels on the CCD, col. 1 lines 13-24).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 5, 10, and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mori et al. in view of Rhodes (US Patent 6,825,878).

Regarding claim 5, Mori et al. teach the solid-state image pickup device according to claim 3. However, Mori et al. do not teach wherein the second voltage is 0 volt.

Rhodes teaches an image sensor using a p-type well (see title) wherein the substrate is biased at a negative voltage by a substrate voltage pump to prevent charge leakage across the transfer gate (col. 5 lines 63-65).

Therefore, it would be obvious to one of ordinary skill in the art to combine the p-type well and negative substrate voltage of Rhodes with the device of Mori et al. so that charge leakage across the transfer gate could be prevented. In such a combination with a negative substrate voltage, a more positive voltage would be required to effect charge transfer from the photodiode region to the vertical register region. Therefore, it would be obvious to apply a more positive voltage such as 0 volts to the transfer gate when the substrate is negatively biased. The examiner also points out that the CCD is a semiconductor device; that the transfer gate is formed as a layer during the semiconductor manufacturing process as shown in Mori Fig. 3; and therefore, the transfer gates can therefore be considered a semiconductor layer. Furthermore, in a semiconductor device such as a CCD, applying a voltage to one layer affects the other layers via electric fields; thus applying a voltage to one layer also applies a voltage to the other layers.

Regarding claims 10 and 24, Mori et al. teach the solid-state image pickup device according to claims 6 and 20. However, they do not teach wherein said well region is a p-type well region and the substrate bias voltage is a negative voltage.

Rhodes teaches an image sensor using a p-type well (see title) wherein the substrate is biased at a negative voltage by a substrate voltage pump to prevent charge leakage across the transfer gate (col. 5 lines 63-65).

Therefore, it would be obvious to one of ordinary skill in the art to combine the p-type well and negative substrate voltage of Rhodes with the device of Mori et al. so that charge leakage across the transfer gate could be prevented.

8. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mori et al. in view of Yanai (US PGPub 2003/0030737).

Regarding claim 11, Mori et al. teach the solid-state image pickup device according to claim 6. However, Mori et al. do not teach wherein said solid-state image pickup device is a complementary metal-oxide semiconductor type solid-state image pickup device which includes a plurality of pixels each of which includes said photoelectric conversion element and a pixel transistor for converting the signal charge read out from said photoelectric conversion element into an electric signal and outputting the electric signal to a signal line.

Yanai teaches an image sensor that may be a CMOS image sensor (par. 84) wherein a substrate voltage is changed so that the amount of charges which may accumulate in pixels is changed to accommodate pixel thinning (see par. 80-84). It is well known in the art that CMOS image sensors inherently comprise a plurality of pixels each of which includes a photoelectric conversion element and a pixel transistor for converting the signal charge read out from said photoelectric conversion element into an electric signal and outputting the electric signal to a signal line.

Therefore, it would be obvious to one of ordinary skill in the art to substitute the CMOS image sensor of Yanai for the CCD image sensor in the pixel-addition method of

Mori et al. so that the image sensor could be integrated with other necessary circuitry such as a timing generator or digital signal processing on a single chip.

9. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Morimoto in view of Rhodes (US Patent 6,825,878).

Regarding claim 17, Morimoto teaches the solid-state image pickup device according to claim 13. However, Morimoto does not teach wherein said well region is a p-type well region and the substrate bias voltage is a negative voltage.

Rhodes teaches an image sensor using a p-type well (see title) wherein the substrate is biased at a negative voltage by a substrate voltage pump to prevent charge leakage across the transfer gate (col. 5 lines 63-65).

Therefore, it would be obvious to one of ordinary skill in the art to combine the p-type well and negative substrate voltage of Rhodes with the device of Morimoto so that charge leakage across the transfer gate could be prevented.

10. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Morimoto in view of Yanai (US PGPub 2003/0030737).

Regarding claim 18, Morimoto teaches the solid-state image pickup device according to claim 13. However, Morimoto does not teach wherein said solid-state image pickup device is a complementary metal-oxide semiconductor type solid-state image pickup device which includes a plurality of pixels each of which includes said photoelectric conversion element and a pixel transistor for converting the signal charge

read out from said photoelectric conversion element into an electric signal and outputting the electric signal to a signal line.

Yanai teaches an image sensor that may be a CMOS image sensor (par. 84) wherein a substrate voltage is changed so that the amount of charges which may accumulate in pixels is changed accordingly (see par. 80-84). It is well known in the art that CMOS image sensors inherently comprise a plurality of pixels each of which includes a photoelectric conversion element and a pixel transistor for converting the signal charge read out from said photoelectric conversion element into an electric signal and outputting the electric signal to a signal line.

Therefore, it would be obvious to one of ordinary skill in the art to substitute the CMOS image sensor of Yanai for the CCD image sensor in the dynamic range increasing method of Mori et al. so that the image sensor could be integrated with other necessary circuitry such as a timing generator or digital signal processing on a single chip.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Tanaka (US Patent 6,982,751) teaches an apparatus similar to Mori et al.

Koizumi et al. (US Patent 7,129,985) teach an image sensing apparatus on a single substrate.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DENNIS HOGUE whose telephone number is (571)270-5089. The examiner can normally be reached on Mon. - Thurs., 8:00 AM - 5:00 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Ho can be reached on (571) 272-7365. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Dennis Hogue/

Examiner, Art Unit 2622

TUAN HO
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